Amendments to the Specification

Please amend paragraph [45] as follows:

[45] The Serdes transceiver chip 400 also includes a management interface 412 that enables the configuration of the portions (parallel ports 102, series port 104, packet BERT 406, and optional logic blocks 408) of the transceiver chip 100. The management interface 412 includes two pads 414 that enable two different management chips to program and control the portions of the transceiver chip 400 using MDIOs blocks 416. For example, one management chip connected to pad 414a could control the parallel port 102a and the serial ports 104a and 104b, and another management chip connected to pad 414b could control the parallel port 102b and the serial ports 104c and 104d. The management interface 412 is configured to be compatible with both IEEE Std. 802.3 clause 45 and the IEEE Std. 802.3 clause 22 management standards. In other words, one management pad 414a and MDIO block 416a can be programmed to be responsive to clause 45 electricals and protocol, and the other management pad 414b and MDIO block 416b could be responsive to clause 22 electricals and protocol. Furthermore, the management pads 414 and MDIO blocks can mix and match clause 22 and clause 45 electrical and protocols. For example, management pad 414a and MDIO block 416a can be responsive to clause 22 electricals and clause 45 protocols, and vice versa. Similar mix and match can be done for the management pad 414b and the MDIO block 416b. The management data pads are further described in U.S. Patent Application No. [[_____]] 10/694,729, titled " Multipurpose and Integrated Pad Ring for Integrated Circuit", filed [[herewith]] October 29, 2003, Attorney Docket No. 1875. 4520000, and U.S. Patent Application No. [[_____]]10/694,730, titled "

Programmable Management I/O Pads for an Integrated Circuit", filed [[herewith]] October 29, 2003, Attorney Docket No. 1875. 4530000, both of which are incorporated by reference herein in its entirety.

Please amend paragraph [51] as follows:

[51] The parallel bus 106 is further described in U.S. Patent Application No.[[_____]] 10/695,485, titled "Cross Link Multiplexer Bus", Attorney Docket No. 1875.3640002, filed [[herewith]] October 29,2003, and incorporated by reference herein in its entirety.